Highly Accurate Dual-Band Cellular Field Potential Acquisition For Brain–Machine Interface

Jing Guo, *Student Member, IEEE*, Jie Yuan, *Member, IEEE*, Jiageng Huang, Jessica Law, Chi-Kong Yeung, and Mansun Chan, *Senior Member, IEEE*

Abstract—Cellular field potential includes local field potential (LFP, 0.1 Hz–200 Hz) and spike potential (SP, 200 Hz–10 kHz). In physiological studies of the brain, SP signal has been the focus. Various circuits have been reported to acquire SP signals in brain–machine interface (BMI) systems over the years. Recent study shows that the LFP signal plays important roles in modulating many profound neuronal mechanisms in the brain. It is important for new BMI design to record the dual-band signal accurately, which demands acquisition circuits to have low noise and good linearity in both bands. In this paper, we report the design of a dual-band acquisition integrated circuit (IC) for microelectrode recording. The novel design uses a continuous-time (CT) front-end with chopping to suppress the noise, and a discrete-time (DT) back-end to achieve good linearity. A prototype monolithic acquisition IC is fabricated in a 0.35 μm CMOS process. It has 16 acquisition channels and an 11 bit successive-approximation (SAR) analog-to-digital converter (ADC). Silicon measurements show that every channel has 29.2 nV/Hz$^{0.5}$ noise and <0.1% nonlinearity. The good linearity effectively prevents the aliasing and mixing between the two bands. For LFP signals, the recording noise is 0.9 μV$_{rms}$. For SP signals, the recording noise is 2.9 μV$_{rms}$. Important to the microelectrode recording, the new design has high input impedance (320 MΩ at 1 kHz), high common-mode rejection ratio (CMRR) (> 110 dB) and power-supply rejection ratio (PSRR) (> 110 dB). Noise-efficiency factor (NEF) of the acquisition channel is 6.6. The IC is experimented with rat cardio-myocytes recording.

Index Terms—Brain–machine interface (BMI), dual-band recording, field potential recording, low-noise front-end.

I. INTRODUCTION

A TYPICAL invasive brain–machine interface (BMI) system is shown in Fig. 1. Microelectrodes sense field potential of neurons in various brain regions. Preamplifiers or more complete acquisition circuits are normally integrated with electrodes to avoid interference on the wire. The acquired signal is processed by external computing devices for physiological or behavioral studies.

Although spikes have long been recognized as playing major roles in neuronal signaling, more and more recent studies find
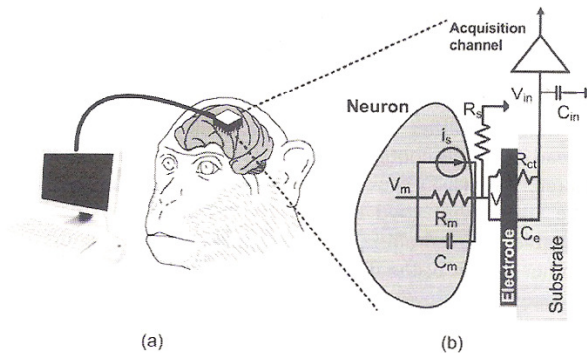
Fig. 1. BMI system diagram.

that LFP modulates a variety of neuronal mechanisms, and plays important roles in various functions, such as memory, attention, and neurological disorders, etc., [1]–[5]. The study on LFP and SP correlation has recently become an active topic in neuroscience. To perform accurate quantitative analysis of the spike field coherence (SFC), it requires the acquisition system to capture the dual-band cellular signal with noise lower than the microelectrode interface noise. Besides low noise in dual bands, good linearity is also needed for the acquisition system to avoid the aliasing and mixing between SP and LFP signals.

The microelectrode interface is critical to the design of BMI. The interface normally features high impedance with noise and high offset [6], [17]. As electrodes are further miniaturized in recent years, higher impedance and noise set more stringent requirements on the acquisition circuits.

Over the years, various bio-potential acquisition circuits have been designed for microelectrodes. Capacitive amplifier front-ends (CAFE) are commonly used in previous designs [6]–[10], [27]. Harrison developed the noise optimization methodology for CAFE in [11]. The design achieved an impressive 2.2 μV$_{rms}$ noise over 7 kHz. This CAFE design inspired a series of biosignal acquisition circuit designs [12]–[15]. Majority of the designs only record the SP signal. The CAFE easily tolerates large electrode offsets and enables high CMRR. Although it works mostly well for SP signals, it has several problems. The CAFE has large low-frequency noise, which is undesirable for LFP signal acquisition. To record the LFP signal, CAFE requires large pseudo-resistor to enable < 1 Hz high pass corner frequency [11]. The signal swing can modulate the pseudo resistance to cause high acquisition nonlinearity (1%). The CAFE also decreases the input impedance of the amplifier. The only acquisition channel designed for dual-band recording was reported in [7], which also used CAFE. As a result, the design

has high noise in the LFP band and low linearity. A CAFE was designed with chopping in [16] for LFP signal acquisition. The low-frequency noise in CAFE is suppressed. The electrode offset is cancelled by feedback, which removes the pseudo-resistor from the signal path. Hence, it achieves low nonlinearity (0.1%). Nonetheless, chopping with CAFE causes low input impedance.

In summary, although quite a few designs have been developed for various bio-potential acquisition systems in recent years, acquisition circuits for dual-band signals with low noise ($< 1\,\mu V_{rms}$), good linearity ($< 0.1\%$) and high input impedance do not exist. In this work, we report such a design. Chopping is used to lower the noise for LFP signal. A new low-noise amplifier is designed to reduce the nonlinearity. Instead of an all-continuous-time (CT) acquisition channel, a discrete-time (DT) back-end is designed to accommodate the large signal with good linearity. Proper filtering is designed to enable sample/hold in the back-end without noise aliasing. Another benefit of the in-channel sample/hold is that it relaxes the design of following multiplexing and quantization circuits. All circuits are fully differential, which achieves good CMRR and PSRR without 50 Hz injection. The input signal is directly applied to a small transistor gate so that the channel input impedance is high. The monolithic acquisition chip includes 16-channels with a successive approximation (SAR) ADC. No external component is needed. The chip is fully verified with biological experiments.

II. MICROELECTRODE–NEURON INTERFACE

The electrode–electrolyte interface is commonly characterized by an interfacial capacitance (C_e) and a charge transfer resistance (R_{ct}) [17]. At the interface in Fig. 1(b), the cell ionic current (i_s) flushes into the gap between the cell membrane and the microelectrode surface, and flows through a seal resistance (R_s) to the reference electrode in the solution. C_{in} is the input capacitance of the acquisition circuit. For normal Au or Pt planar microelectrodes with tens of μm diameter, C_e is about hundreds of pF, and R_{ct} is about several hundred MΩ [6], [12], [17]. The surface capacitance of Pt-black microelectrodes can be 10 times larger. R_s varies significantly from hundreds of $k\Omega$ to MΩ depending on the distance between the neuron and the electrode surface [18], [19].

The interface noise comes from both $R_{ct}(i_{n,rct})$ and $R_s(i_{n,s})$. It can be derived that the R_{ct} noise is low-pass filtered to the amplifier input as

$$v_{n,in,rct} = \frac{R_{ct}}{(sR_{ct}C_e + 1)(sR_sC_{in} + 1)} i_{n,rct}. \quad (1)$$

The corner $1/(2\pi R_{ct}C_e)$ is usually low in the Hz range for planar micro-electrode, while the corner $1/(2\pi R_sC_{in})$ is usually much higher than the cellular signal band. Hence, in the cellular signal band, the R_{ct} noise has a low frequency corner $1/(2\pi R_{ct}C_e)$. The overall noise power from R_{ct} is independent of R_{ct} as $(kT/C_e)^{0.5}$. It can also be derived that the R_s noise is bandpass filtered to the amplifier input as

$$v_{n,in,rs} = \frac{sR_sC_{in}R_{ct}}{(sR_{ct}C_e + 1)(SR_sC_{in} + 1)} i_{n,rs}. \quad (2)$$
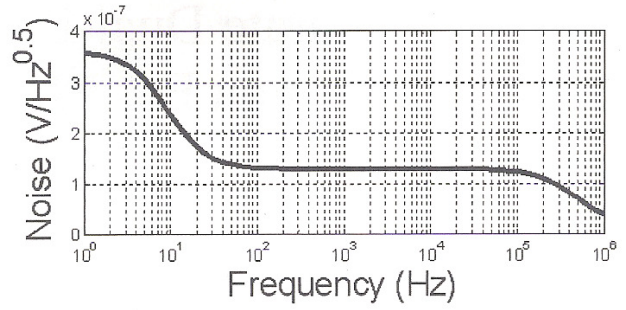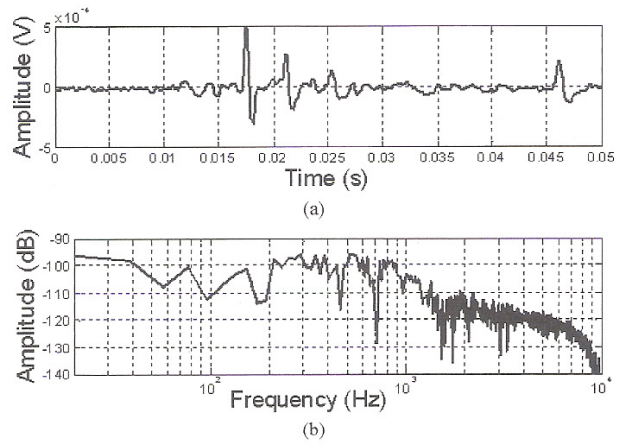

Fig. 2.   Simulated interface noise.

Fig. 3.   (a) Recorded neuron field potential. (b) Spectrum.

This is a wide band noise. Hence, the overall in-band interface noise power is

$$V_{n,in} = \sqrt{4kTR_s \cdot \Delta f + \frac{kT}{C_e}} \quad (3)$$

where Δf is the acquisition circuit bandwidth. This result is similar to common results derived in previous work [20]–[22] with the difference that the low-pass R_{ct} noise is integrated. Fig. 2 plots the simulated interface noise for a planar Pt-black electrode with 20 μm in diameter ($R_{ct} = 6.8\,M\Omega$, $C_e = 3nF$) and a seal resistance $R_s = 1\,M\Omega$. Within the LFP band, the noise power is $2.1\,\mu V_{rms}$ including $1.1\,\mu V_{rms}$ from R_{ct} and $1.8\,\mu V_{rms}$ from R_s. Within the 10 kHz cellular signal band, the noise power is $12.9\,\mu V_{rms}$. R_s noise dominates. The wideband noise density is $129\,nV/Hz^{0.5}$. If the neuron is farther away from the electrode, R_s can be much smaller, which causes less in-band noise. Hence, the BMI acquisition channel desires to achieve noise power $<1\,\mu V_{rms}$ (LFP band) and $<5\,\mu V_{rms}$ (SP band) with noise density $<50nV/Hz^{0.5}$ in the cellular signal band.

BMI microelectrode can experience field potential up to 10 mV. Field potential recorded from an individual neuron usually has high SP component, while field potential recorded from group of neurons has high LFP component [16]. If the acquisition circuit is nonlinear, the SP signal can alias into the LFP band through self-mixing or the LFP signal harmonics can
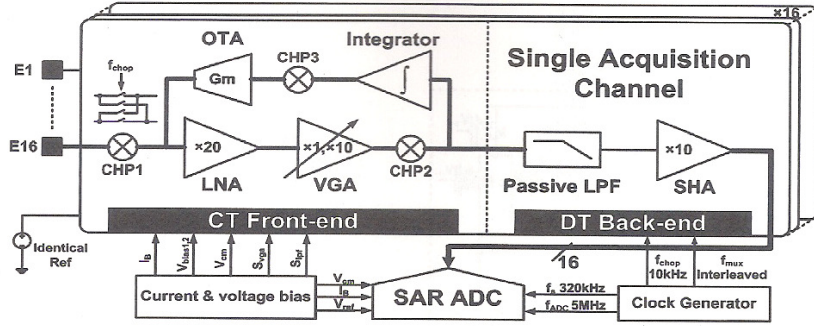
Fig. 4. Acquisition IC system diagrams.

alias into the SP band. A typical recording of dissociated rat hippocampal neurons and its spectrum are shown in Fig. 3 [10]. Its signal energy mainly locates in the range 200 Hz–1 kHz. If the acquisition channel has 1% nonlinearity, which are equally contributed by HD2 and HD3, the aliased SP signal into the LFP band is $1.2\,\mu V_{rms}$. If the nonlinearity is reduced to 0.1%, the aliased SP signal is $0.12\,\mu V_{rms}$. To limit the distortion lower than the noise within the $20\,mV_{pp}$ signal range, a dual-band acquisition channel requires <0.1% nonlinearity.

III. CIRCUIT DESCRIPTION

Architecture of the dual-band BMI signal acquisition chip is shown in Fig. 4 in a 0.35 μm CMOS process. It includes 16 channels and one SAR ADC for quantization. Every channel samples at 20 kS/s. The 11-bit SAR ADC quantizes the multiplexed channel outputs at the rate of 320 kS/s.

Each channel includes a CT front-end and a DT back-end. Circuits in the CT front-end are optimized for both noise and linearity. The front-end has variable gains (26 dB, 46 dB). To acquire the LFP signal, the front-end performs chopping at 10 kHz to achieve lower noise. Similar to [23], the electrode offset is cancelled by a feedback in the front-end. Circuits in the DT back-end are optimized for linearity. It further amplifies the signal by 20 dB.

A. Low Noise Amplifier

To achieve high input impedance for the acquisition channel, a source degenerated low-noise amplifier (LNA) as shown in Fig. 5 is designed at the channel front. The feedback with $M1 \sim 5$ drives the M1 source to follow the input voltage V_{in}. The AC current in R_1 resistor is split between M1 and M5. The useful portion is mirrored by $M_{5,6}$ to generate the output signal V_o on R_2. Hence, the amplifier midband gain is

$$A_{md,\ln a} = \frac{R_2}{R_1} \cdot \frac{S_6}{S_5} \cdot \frac{1}{1 + \frac{i_{m1}}{i_{m5}}} \qquad (4)$$

where S6/S5 is the size ratio of M6 and M5. i_{m5}/i_{m1} is the AC current split ratio between M5 and M1. To achieve good amplifier linearity, this current split ratio needs to be large and independent of the input signal. The current split ratio at low frequency can be derived as

$$\frac{i_{m5}}{i_{m1}} = \frac{S_5}{S_4} \frac{g_{m1}}{g_{m1} + g_1} \frac{g_{m3} r_A}{1 + \frac{g_{m3}}{g_{m4}}} \qquad (5)$$
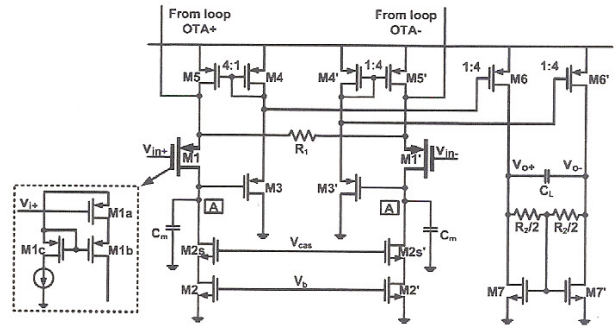

Fig. 5. Low-noise amplifier circuit diagram.

where S5/S4 is the size ratio of M5 and M4. g_1 is the conductance of R1. r_A is the output resistance at node A. Compared to the LNA in [23], the current split ratio in the new design is larger. Also, poles in the new feedback loop are higher in frequency, which can keep high current split ratio even at high frequencies. The V_{ds} of M1,1' are clamped to keep g_{m1} independent of the signal. Both R1 and R2 are poly resistors for good linearity. With this LNA, high linearity (-70.6 dB THD, total harmonic distortion) is achieved for $20\,mV_{pp}$ signal. The LNA gain is 26 dB.

The LNA thermal noise is mainly contributed by M1,2,5,6 and R1. Its input-referred noise density can be derived as

$$\overline{dv_{n,\ln a}^2} = \frac{16kT}{3} \left[\frac{1}{g_{m1}} + \frac{3}{4g_1} + \frac{g_{m5}}{g_1^2} + \frac{g_{m6}}{g_1^2} + \frac{g_{m2}}{(g_{m1}//2g_1)^2} \right] df \qquad (6)$$

g_{m1} and g1 are increased to suppress the LNA noise down to $24.7\,nV/Hz^{0.5}$ at 10 kHz. The LNA power is 40.1 μW, which has 4.14 NEF [11].

B. Variable Gain Amplifier and Front-End Feedback

To further suppress the low-frequency noise from the back-end, the front-end includes a capacitive variable gain amplifier (VGA) as shown in Fig. 6. The VGA midband gain is set by the capacitor ratio to be 0 dB or 20 dB. Its close-loop bandwidth is designed to enable the low-pass cut-off frequency at 30 kHz. The THD of this capacitive VGA for $400\,mV_{pp}$ input signal is -70.6 dB.
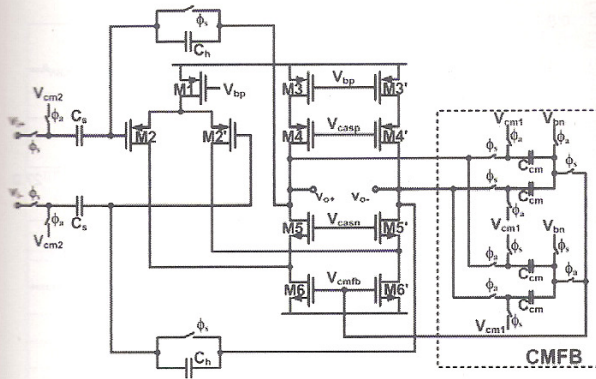
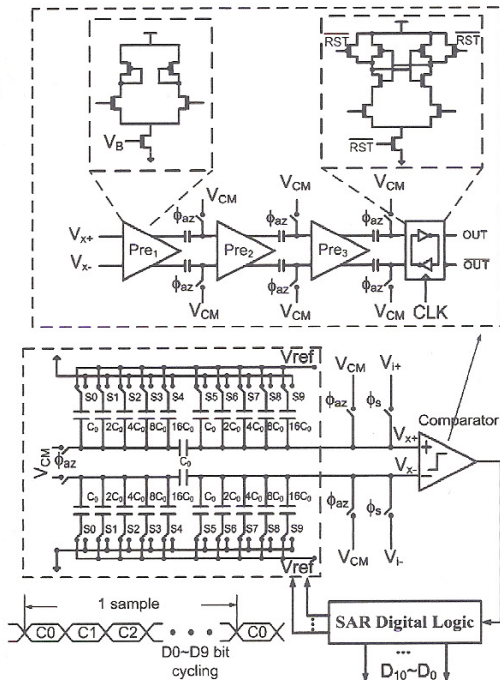Fig. 10. Switched-capacitor back-end amplifier.

Fig. 11. The 11-bit 320 kS/s SAR ADC block diagram.

300 fF unit capacitor is needed to enable 11-bit linearity for our process. The comparator includes three preamplifiers with auto-zeroing to suppress the latch noise lower than 1/4 LSB ($LSB = 1.96$ mV). The pre-amplifier gain is 3. Within the auto-zeroing cycle (C0), the bridging capacitor is reset and the pre-amplifier offsets are sampled. In D_{10} cycle (C1), the differential input signal is compared to determine the most significant bit (MSB) D_{10}. In the sampling cycle (C2), the capacitor array is charged with either the positive reference ($V_{ref}, 0$) or negative reference ($0, V_{ref}$) based on D_{10}. The common bit cycling procedure follows to resolve the remaining 10 bits.

IV. IMPLEMENTATION AND MEASUREMENTS

The micrograph of the fabricated die is shown in Fig. 12. It includes 16 acquisition channels, a SAR ADC, reference gen-
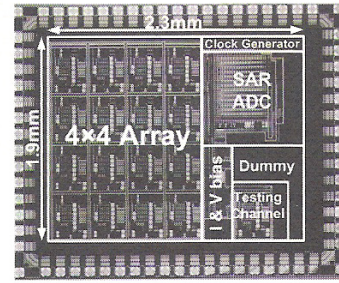

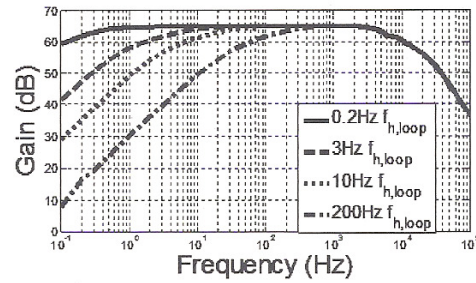Fig. 12. Die micrograph 1.9mm × 2.3mm.

Fig. 13. The measured channel gain at 66 dB gain mode.

eration circuits and a testing channel. Every channel's size is $480\ \mu m \times 320\ \mu m$. The SAR ADC's size is $800\ \mu m \times 800\ \mu m$. In the layout, poly capacitors occupy large area. The channel size can be reduced significantly by laying the active circuits under the metal–insulator–metal (MIM) capacitors.

A. Acquisition Channel

The channel gain is measured by applying sinusoidal signal with different frequencies to the channel. In the high-gain mode, the measured channel gain is shown in Fig. 13. The high-pass corner can be tuned to < 0.1 Hz. To acquire the SP signal, the corner is tuned to 200 Hz. Similar frequency tuning is available for the low gain (46 dB) mode.

The measured channel noise density is shown in Fig. 14. For SP signal acquisition, chopping is not applied. The measured thermal noise density is $29.2\ \mathrm{nV/Hz}^{0.5}$. The noise in the SP band is $2.9\ \mu V_{rms}$. The noise corner extends to 100 Hz. The 1/f noise dominates the LFP band. To acquire LFP signals, chopping is applied. The noise corner is cut to 20 Hz. The noise in the LFP band reduces to $0.9\ \mu V_{rms}$. Each channel consumes $74\ \mu W$ power, which leads to the channel NEF to be 6.6.

The channel linearity is measured by applying a $20\ \mathrm{mV_{pp}}214$ Hz sinusoidal signal to the channel. The output spectrum is shown in Fig. 15. The channel is dominated by HD3. The THD is -59.6 dB. Equivalently, the nonlinearity is about 0.1%. This nonlinearity stays similar with and without chopping. The CMRR and PSRR of every channel are measured. Due to the fully differential design, both CMRR and PSRR are beyond 110 dB. No 50 Hz injection has been observed in chip measurements. The only occasion that 50 Hz signal is observed is when signal wires in the biological measurement are not properly shielded.
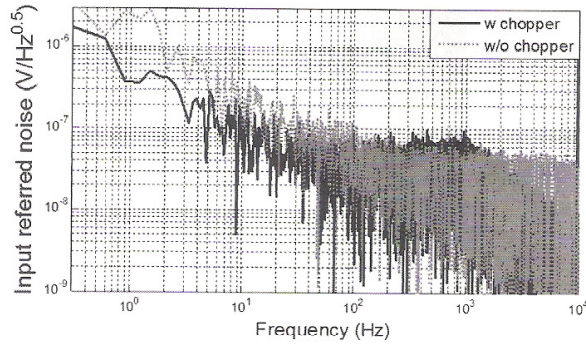
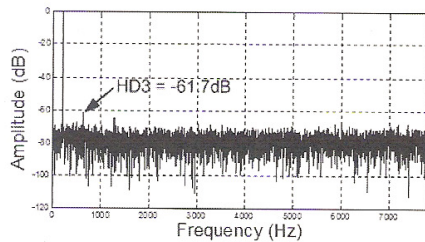Fig. 14. Measured channel noise with and without chopping.

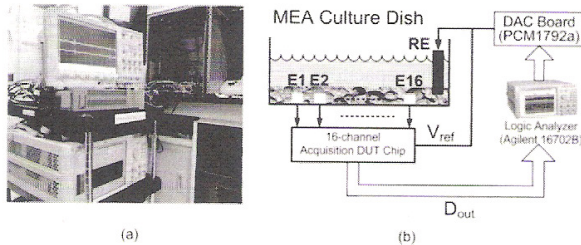Fig. 15. Recorded spectrum for channel linearity measurement.

Fig. 16. Rat cardiac-myocytes recording setup.

Fig. 17. (a) Zoom-in spike. (b) Recorded cardiomyocytes SP signal. (c) Recorded cardiomyocytes LFP signal.

B. In Vitro Biological Recording

The prototype chip is bonded with planar microelectrodes to test under *in vitro* physiological conditions. The gold micro-electrode size is $20~\mu\mathrm{m} \times 20~\mu\mathrm{m}$. A photo of the experiment setup is shown in Fig. 16(a) with the system diagram shown in Fig. 16(b). Dissociated cardiomyocytes from embryonic days 16–19 Sprague–Dawley rats are used to test the acquisition setup. The cardiomyocytes can initiate field potentials without external stimulation.

The sample is prepared following the procedure described in [25], [26]. With the chopping disabled, the acquisition chip digitizes the field potential. The digitized signal is further filtered by a software filter to select the SP signal. A typically recorded SP signal is plotted in Fig. 17(b). The signal intensity is $13.5~\mu\mathrm{V_{rms}}$. A zoomed-in voltage spike is shown in Fig. 17(a). With the chopping enabled and the 1 kHz low-pass filter, the LFP signal can be aquired. A typically recorded LFP signal is shown in Fig. 17(c). The signal intensity is $48.4~\mu\mathrm{V_{rms}}$. If the signals are acquired by circuits with 0.1% nonlinearity equally contributed by HD2 and HD3, the mixed signal component
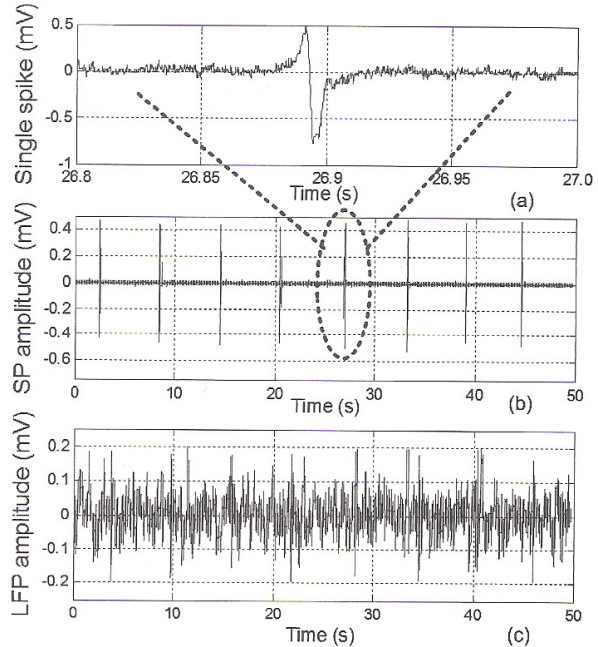
aliased into the LFP band is $0.1~\mu\mathrm{V_{rms}}$. Therefore, the high linearity keeps the signal distortion lower than its noise. As cardiomyocytes have lower pulse rate than neurons, the rms signal intensity is weaker. With stronger signal, the distortion component can be more significant.

The overall performance of the dual-band acquisition chip is summarized and compared with previous benchmark designs in Table I. Compared to previous bio-signal acquisition circuits, this design generally achieves much improved noise and linearity. It enables dual-band recording. It also has much larger input impedance, which is important for smaller electrodes. The design also has excellent CMRR and PSRR. Due to the low noise and good linearity, the new design achieves wider dynamic range compared to previous designs. Its NEF is comparable to other designs.

V. CONCLUSION

New BMI requires the accurate recording of both LFP and SP signals. This demands the acquisition circuits to have low noise and good linearity throughout the cellular signal band. In this work, we designed a new architecture for dual-band field-potential acquisition. A continuous-time front-end with chopping achieves low noise in the LFP band, while a discrete-time back-end achieves good linearity.

A monolithic acquisition chip including 16 channels is fabricated in a $0.35~\mu\mathrm{m}$ CMOS process. Each channel has tunable gain (46 dB, 66 dB) and tunable high-pass corner. With chopping, each channel has $0.9~\mu\mathrm{V_{rms}}$ noise in the LFP band. Without chopping, the channel has $2.9~\mu\mathrm{V_{rms}}$ noise in the SP band. The channels have 0.1% nonlinearity. Due to the fully-differential design, the channels have CMRR and PSRR beyond

TABLE I
PERFORMANCE COMPARISON WITH BENCHMARK BIO-POTENTIAL ACQUISITION DESIGNS

	[11]	[6]	[7]	[15]	[10]	[24]	[16])	this work
Gain	40dB	60dB, 70dB	54-74dB	48-68dB	0-80dB (18 steps)	72-82dB	41, 50.5dB	46, 66dB
Input impedance @1kHz	8MΩ (20pF)	80MΩ (2pF)	-	32MΩ (5pF)	-	>1000MΩ	8MΩ	320MΩ 100MΩ(chopping)
THD	1% 16.7mV input	0.25% 1mV input	1% 1V output	0.7% 4.4mV input	-	<1% 0.4mV input	<0.1% 5mV input	0.1% 20mV input
Noise	$292nV/Hz^{0.5}$ (0.014-30Hz) $26nV/Hz^{0.5}$ (0.025-7.2k Hz)	$5.9\mu V_{rms}$ (10-100kHz) $67nV/Hz^{0.5}$	$10\mu V_{rms}$ LFP (<350Hz) $3\mu V_{rms}$ for SP (350Hz-10kHz)	$7\mu V_{rms}$ (5kHz) $100nV/Hz^{0.5}$	$2.4\mu V_{rms}$ (1-100kHz) $27nV/Hz^{0.5}$ (cal)	$0.59\mu V_{rms}$ (0.5-100 Hz) $59nV/Hz^{0.5}$	$0.98\mu V_{rms}$ (0.05-100Hz) $98nV/Hz^{0.5}$	$64nV/Hz^{0.5}$ (1-200 Hz) $29.2nV/Hz^{0.5}$ (200Hz-10kHz)
Dynamic Range	69dB for both	42dB	44-56dB	53dB (cal)	-	48dB (cal)	71dB (cal)	78dB for LFP 69dB for SP
CMRR	>83dB	70dB	90dB	-	-	>120dB	>100dB	>110dB
Power	$0.9\mu W$ $80\mu W$	$160\mu W$	$75\mu A$	$15\mu W$	$160\mu W$	$6.9\mu W$	$1.8\mu W$	$74\mu W$
NEF	4.8 and 4.0 (single amp)	18.1 (cal)	10.4	4.6 (single amp)	7.4 (cal)	4.3	4.6	4.1 (LNA) 6.6
Area	$0.22mm^2$ $0.16mm^2$	$0.06mm^2$	$0.08mm^2$	$0.04mm^2$	$0.07mm^2$	$0.45mm^2$	$1.7mm^2$	$0.15mm^2$
Technology	$1.5\mu m$	$0.6\mu m$	0.35mm	$0.35\mu m$	$0.6\mu m$	$0.5\mu m$	$0.18\mu m$	$0.35\mu m$
Supply Voltage	±2.5V	5V	-	3V	5V	3V	1.8V	3.3V

110 dB without the 50 Hz injection. The chip has high input impedance of 320 MΩ at 1 kHz.

Compared to previous bio-potential acquisition circuit designs, the new design has advantages on noise and linearity, which leads to wider dynamic range. It also has high CMRR, PSRR and input impedance, which are important for BMI electrodes. Overall, the new design is the first design to enable high-quality dual-band recording.

REFERENCES

[1] N. Klauke, G. Smith, and J. Cooper, "Extracellular recordings of field potentials from single cardiomyocytes," *Biophys. J.*, vol. 91, pp. 2543–2551, Oct. 2006.

[2] S. Reichinnek, T. Kunsting, A. Draguhn, and M. Both, "Field potential signature of distinct multicellular activity patterns in the mouse hippocampus," *J. Neurosci.*, vol. 46, pp. 15441–15449, Nov. 2010.

[3] U. Rutishauser, I. Ross, A. Mamelak, and E. Schuman, "Human memory strength is predicted by theta-frequency phase-locking of single neurons," *Nature*, vol. 464, pp. 903–909, Apr. 2010.

[4] P. Fries, J. Reynolds, A. Rorie, and R. Desimone, "Modulation of oscillatory neuronal synchronization by selective visual attention," *Science*, vol. 291, pp. 1560–1563, Feb. 2001.

[5] D. W. Grasse and K. A. Moxon, "Correction the bias of spike field coherence estimators due to a finite number of spikes," *J. Neurophysiol.*, vol. 104, pp. 548–558, May 2010.

[6] F. Heer, S. Hafizovic, W. Franks, A. Blau, C. Ziegler, and A. Hierlemann, "CMOS microelectrode array for bidirectional interaction with neuronal networks," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1620–1629, Jul. 2006.

[7] Y. Perelman and R. Ginosar, "An integrated system for multichannel neuronal recording with spike/LFP separation, integrated A/D conversion and threshold detection," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 1, pp. 130–137, Jan. 2007.

[8] R. A. Blum, J. D. Ross, E. A. BrownStephen, and P. DeWeerth, "An integrated system for simultaneous, multichannel neuronal stimulation and recording," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 54, no. 12, pp. 2608–2618, Dec. 2007.

[9] M. Chae, W. Liu, and M. Sivaprakasam, "Design optimization for integrated neural recording systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1931–1938, Sep. 2008.

[10] U. Frey, J. Sedivy, F. Heer, R. Pedron, M. Ballini, J. Mueller, D. Bakkum, S. Hafizovic, F. Faraci, F. Greve, K. Kirstein, and A. Hierlemann, "Switch-matix-based high-density microelectrode array in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 467–482, Feb. 2010.

[11] R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[12] R. Olsson and K. Wise, "A three-dimensional neural recording microsystem with implantable data compression circuitry," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2796–2804, Dec. 2005.

[13] R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.

[14] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 6, pp. 136–147, Jun. 2007.

[15] J. Aziz, K. Abdelhalim, R. Shulyzki, R. Genov, B. Bardakjian, M. Derchansky, D. Serletis, and P. Carlen, "256-channel neural recording and delta compression microsystem with 3D electrodes," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 995–1095, Mar. 2009.

[16] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley, and A. Kelly, "A 2uW 100 nV/Hz chopper-stabilized instrumentation amplifier for chronic measurement of neural filed potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[17] A. David, "Cell based biosensors using microelectrodes," Ph.D. dissertation, Standford Univ., Stanford, CA, 1998.

[18] J. Buitenweg, W. Rutten, and E. Marani, "Geometry-based finite-element modeling of the electrical contact between a cultured neuron and a microelectrode," *IEEE Trans. Biomed. Eng.*, vol. 50, no. 4, pp. 501–509, Apr. 2003.

[19] S. Ingebrandt, C.-K. Yeung, M. Krause, and A. Offenhausser, "Neuron-transistor coupling: Interpretation of individualextracellular recorded signals," *Eur Biophys J.*, vol. 34, pp. 144–154, 2005.

[20] F. Heer, W. Franks, A. Blau, S. Taschini, C. Ziegler, A. Hierlemann, and H. Baltes, "CMOS microelectrode array for monitoring of electrogenic cells," *Biosens. Bioelectron.*, vol. 20, pp. 358–366, Mar. 2004.

[21] C. D. James, A. J. H. Spence, N. M. Dowell-Mesfin, R. J. Hussain, K. L. Smith, H. G. Craighead, M. S. Isaacson, W. Shain, and J. N. Turner, "Extracellular recordings from patterned neuronal networks using planar microelectrode arrays," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 9, pp. 1640–1648, Sep. 2004.

[22] N. Joye, A. Schmid, and Y. Leblebici, "A cell-electrode interface noise model for high-density microelectrode arrays," in *IEEE EMBS Conf.*, Sep. 2009, pp. 3247–3250.

[23] R. Yazicioglu, P. Merken, and C. Van Hoof, "A 60uW 60 nV/Hz readout front-end for portable biopotential acquisition systems," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, May 2007.

[24] R. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 200uW eight-channel EEG acquisition ASIC for ambulatory EEG systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3039, Dec. 2008.

[25] C.-K. Yeung, F. Sommerhage, G. Wrobel, J. K.-Y. Law, A. Offenhäusser, J. A. Rudd, S. Ingebrandt, and M. Chan, "To establish a pharmacological experimental platform for the study of cardiac hypoxia using the microelectrode array," *J. Pharmacol. Toxicol. Methods*, vol. 59, pp. 146–152, 2009.

[26] J. K. Y. Law, C. K. Yeung, K. L. Yiu, J. A. Rudd, S. Ingebrandt, and M. Chan, "A study of the relationship between pharmacology preconditioning and adenosine triphosphate-sensitive potassium (KATP) channels on cultured cardiomyocytes using the microelectrode array," *J. Cardiovasc. Pharmacol. TM 56*, pp. 60–68, 2010.

[27] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower CMOS integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 1, pp. 1–10, Feb. 2009.

[28] L. Jongwoo, M. D. Johnson, and D. R. Kipke, "A tunable biquad switched-capacitor amplifier-filter for neural recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 5, pp. 295–300, Oct. 2010.

Jing Guo (S'09) received the B.S. degree in electronic science and technology from Shanghai Jiao Tong University, Shanghai, Beijing, China, in 2007 and the M.S. degree in integrated circuit design, in 2009, from the Hong Kong University of Science and Technology (HKUST), Kowloon, Hong Kong, where she is currently working toward the Ph.D. degree.

Her research interest is on developing the high performance bio-sensory circuits for biomedical applications, including low-noise and high linearity mixed-signal IC design and device fabrication.

Jie Yuan (S'03–M'06) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2000, and the Ph.D. degree in electrical engineering from University of Pennsylvania, Philadelphia, in 2006.

Since 2006, he has been an Assistant Professor in the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology. His research interest is on high-performance mixed-signal IC design for bio-medical applications. More specific research interests of his group include ultra low-power data converters, high-performance analog front-ends, and CMOS imaging sensors for medical diagnostics.

Dr. Yuan served as the Technical Program Committee Co-Chair of IEEE Biomedical Circuits and Systems Conference 2009. He was a Guest Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS. He is a technical committee member of the IEEE Symposium on Circuits and Systems. He also serves as the Vice Chair of the Biomedical Circuits and Systems Technical Committee. He is the Finance Chair of the IEEE VLSI-SOC conference.

Jiageng Huang received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2009. He is currently working toward the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Kowloon, Hong Kong.

In 2009, he joined the Mixed-Signal Bio-Medical Integrated Circuits Laboratory, the Hong Kong University of Science and Technology (HKUST). His research areas include SAR ADC, continuous time Sigma-Delta ADC, and ultrasound front-end circuits.

Jessica Ka-Yan Law received the B.Sc. degree from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2005, and the M.Phil. and Ph.D. degrees from The Chinese University of Hong Kong and The Hong Kong University of Science and Technology (HKUST), in 2007 and 2011, respectively.

She has more than four years of experience in working with international scholars in the field of microelectrode arrays. She had been a visiting researcher to Forschungszentrum Jülich, Germany and University of Applied Sciences Kaiserslautern, Germany. Her research interests include development of drug-screening biosensor and microelectrode array chips. Currently, she is a postdoctoral researcher in HKUST.

Chi-Kong Yeung the B.Sc. degree in biomedical sciences and the Ph.D. degree in pharmacology and physiology from University of Bradford, Bradford, U.K., in 1993 and 1996, respectively.

He is a Member of the Institute of Biomedical Science, a Chartered Biologist, and a Fellow of the Society of Biology. He is currently an Adjunct Associate Professor in the School of Biomedical Sciences at the Chinese University of Hong Kong. His research interests are neuronal plasticity, cardiovascular pathophysiology, and gastrointestinal functions.

Mansun Chan (SM'11) received the B.S. degree from the University of California (UC), San Diego, in 1991 and the M.S. and Ph.D. degrees from the UC, Berkeley, in 1994 and 1995, respectively.

His research at UC Berkeley covered a broad area in silicon devices ranging from process development to device design, characterization, and modeling. A major part of his work was on the development of record breaking silicon-on-insulator (SOI) technologies. He has also maintained a strong interest in device modeling and circuit simulation. He is one of the major contributors to the unified BSIM model for SPICE, which has been accepted by most semi-conductor companies and the Compact Model Council (CMC) as the first industrial standard metal-oxide—semiconductor field-effect transistor model. Since 1996, he has been with the Electrical and Electronic Engineering faculty, The Hong Kong University of Science and Technology, Kowloon, Hong Kong. Between July 2001 and December 2002, he was a Visiting Professor with the UC Berkeley and the Co-Director of the BSIM program. His research interests include nanodevice technologies, image sensors, SOI technologies, high-performance integrated circuits, 3-D circuit technology, device modeling, and nano biomedical nano-electro-mechanical-systems technology.